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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,755	09/17/2003	Sterling Smith	MSS0007-US	3830

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EXAMINER	
NGUYEN, HIEP	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 09/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/663,755	SMITH, STERLING	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The finality of the Office Action filed on 02-01-06 has been withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3 and 4 are rejected under 35 U.S.C.102 (b) as being anticipated by Peterson et al. (US pat. 5,926,217).

Regarding claim 1, figures 3, 4 and 5c show an interface circuitry of a display chip comprising: an input node receiving an analog input signal from the output of infrared image sensor (111); an adjustable filter (117, col.1, lines 59-61) providing a bandwidth in response to a display mode; a clamping circuit (131) for clamping the processed image signal during a clamping interval. One of ordinary skill in the art knows that that the low-pass filter basically filters out the unwanted high frequencies or high frequency noises. By varying the value of the resistor (RC value), the bandwidth of the filter varies. The bandwidth of the filter contents a spectrum of frequencies i.e., a range of information including video display information. By varying the bandwidth of the filter the display resolution varies. Therefore, this is an inherent feature of any adjustable filter (see USP. 6,606,171 and US. 6,738,087).

Regarding claims 3 and 4, the clamping circuit (131) comprises transistor (M9). The connection of the clamp circuit is shown in figure 3.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in

the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peterson et al. (US pat. 5,926,217) in view Renk et al. (US. 6,606,171).

Regarding claim 1, figures 3 and 4 of Peterson shows an interface circuitry of a display chip comprising: an input node receiving an analog input signal from the output of infrared image sensor (111); an adjustable filter (117, col.1, lines 59-61) providing a bandwidth in response to a display mode; a clamping circuit (131) for clamping the processed image signal during a clamping interval. Peterson does not disclose that the adjustable filter (117) provides a bandwidth adjustable in response to the display resolution such that the greater the display resolution, the greater the bandwidth. Figures 19 and 20 of Renk show a video circuit receiving image signal having an adjustable filter for providing a bandwidth adjustable in response to the display resolution such that the greater bandwidth the greater the display resolution (col.18, lines 48-55; col. 19, lines 56-66). Note that the resolution is a function of the bandwidth. If the bandwidth is narrow, the resolution (image brightness) is smaller (col. 18, lines 53-55).

Regarding claim 2, figure 4 of Peterson shows the detailed circuit of the adjustable low-pass filter (117) having a variable resistor comprising elements (D2, D3, M3). Diode (D2) acts as a variable resistor that is adjusted by diode (D3) and transistor (M3), (col.6, lines 41- 50).

Regarding claims 3 and 4, figure 4 shows the clamping circuit (131) comprising a transistor (M9). The clamping signal is signal (VCLMP).

Regarding claims 5 and 6, the variable resistor variable resistor comprises elements (D2, D3, M3). The connection of transistor (M9) and resistor is clearly shown in figures 3 and 4 of Peterson.

Claims 7-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Obie et al. (US Pat. 5,038,096) in view Peterson et al. (US pat. 5,926,217), Renk et al. (USP. 6,606,171), Kanagawa (6,366,866) and Kwon (6,724,245).

Regarding claim 7, figure 1 of Obie shows an interface circuitry of a display chip comprising;

an input node for receiving an analog image signal with a display resolution; note that every video signal has a display resolution.

a video filter (112) for processing said analog image signal and providing a processed image signal at internal node;

an ADC unit (118) for converting said processed image signal into a digital image signal.

Figure 1 of Obie does not show a clamping circuit connecting between said internal node and a reference level and the filter is adjustable. Figures 3 and 4 of Peterson show a clamping circuit (131) for clamping the node voltage with a reference voltage during clamping interval for enhancing the signal to noise ratio (col. 60-65) Therefore, it would have been obvious to one of ordinary skill in the art to implement the clamping circuit taught by Peterson to the circuit of Obie for enhancing the signal to noise ratio. Figure 1 of Obie does not show that the low-pass filter is adjustable filter for providing a bandwidth adjustable in response to the display resolution such that the greater the display resolution. Figures 19 and 20 of Renk shows a video circuit receiving image signal having an adjustable filter for providing a bandwidth adjustable in response to the display resolution such that the greater the bandwidth, the greater the display resolution (col.18, lines 48-55; col. 19, lines 56-66). Therefore, it would have been obvious to one of ordinary skill in the art to replace the filter (112) of Obie with the adjustable filter taught by Renk for providing a bandwidth adjustable in response to the display resolution such that the greater the bandwidth, the greater the display resolution.

Regarding claim 8, the combination of Obie, Peterson and Renk includes all the limitations of claim 8 except for the limitation that the low pass filter (112) of Obie comprises a variable resistor. Note that the low-pass filter of the present application in figures 2 and 3 of the present application is a simple low-pass filter comprising two elements: a variable resistor and a capacitor. One of ordinary skill in the art know that a low-pass filter is used in any analog circuit including video circuit for eliminating unwanted frequencies or to vary the resolution of the display (See US 6,606,171; US 6,738,087). The bandwidth of the low-pass

filter depends on the (R-C) values of the resistor and the capacitor that determine the cut-off frequency or the bandwidth of the low-pass filter.

As discussed above, figure 3 of Kanagawa shows an adjustable low-pass filter (211), similar to the simple low-pass filter low-pass filter (24) of the present application in figures 2 and 3 of the present application, comprising a variable resistor (2111) and (2112) for varying the bandwidth of the low-pass filter thus, the resolution of the analog signal or the video signal is adjustable (smaller or greater). Therefore, it would have been obvious to one of ordinary skill in the art to consider that the adjustable filter (112) of Obie comprises a variable resistor as taught by Kanagawa for varying the bandwidth of the filter.

Regarding claims 9 and 10, the clamping circuit (131) taught by Peterson (131) for clamping the node voltage with a reference voltage during clamping interval for enhancing the signal to noise ratio (col. 60-65) comprises a transistor (M9) having a drain connected to the internal node and a source connected to a reference level.

Regarding claims 11 and 12, the combination of Obie, Peterson, Renk and Kanagawa includes all the limitation of claim 10 except for the limitation that the clamping circuit comprises a variable resistor and a transistor. Figure 1 of Kwon shows a clamping circuit comprising a variable resistor (N1) control by signal (Vbias) and a clamping transistor (N2) controlled by signal (clamp_en) for adjusting the voltage at the internal node (col. 5, lines 12-33). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the clamping circuit taught by Kwon to the circuit of Obie for adjusting the voltage at the internal node. The connections of these two components are clearly shown in figure 1 of Kwon.

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peterson et al. (US. 5,926,217) in view Belkin et al. (US. 6,738,087).

Regarding claim 1, figures 3 and 4 of Peterson shows an interface circuitry of a display chip comprising: an input node receiving an analog input signal from the output of infrared image sensor (111); an adjustable filter (117, col.1, lines 59-61) providing a bandwidth in response to a display mode; a clamping circuit (131) for clamping the processed image signal during a clamping interval. Peterson does not disclose that the adjustable filter

(117) provides a bandwidth adjustable in response to the display resolution such that the greater the display resolution, the greater the bandwidth. Figure 1of Belkin shows a video circuit receiving image signal having an adjustable filter (2) for providing a bandwidth adjustable in response to the display resolution such that the greater the bandwidth, the greater the display resolution (col.1, lines 40-67). Therefore, it would have been obvious to on of ordinary skill in the art to replace the adjustable filter (117) of Peterson with the adjustable filter of Belkin for providing a bandwidth adjustable in response to the display resolution such that the greater the bandwidth, the greater the display resolution. Note that Belkin discloses that a picture having a resolution of 354 times 288 pixels corresponds to a high frequency of 20,340,400 Hertzs. This frequency is too high for the conventional phone line frequency. In order to reduce the frequency, the resolution must be reduced. Therefore, the resolution is proportional to the bandwidth.

Regarding claim 2, figure 4 of Peterson shows the detailed circuit of the adjustable low-pass filter (117) having a variable resistor comprising elements (D2, D3, M3). Diode (D2) acts as a variable resistor that is adjusted by diode (D3) and transistor (M3), (col.6, lines 41- 50).

Regarding claims 3 and 4, figure 4 shows the clamping circuit (131) comprising a transistor (M9). The clamping signal is signal (VCLMP).

Regarding claims 5 and 6, the variable resistor variable resistor comprises elements (D2, D3, M3). The connection of transistor (M9) and resistor is clearly shown in figures 3 and 4 of Peterson.

Claims 7-12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Obie et al. (US Pat. 5,038,096) in view Peterson et al. (US pat. 5,926,217), Belkin et al. (USP. 6,738,087), Kanagawa (6,366,866) and Kwon (6,724,245).

Regarding claim 7, figure 1 of Obie shows an interface circuitry of a display chip comprising:

an input node for receiving an analog image signal with a display resolution; note that every video signal has a display resolution.

a video filter (112) for processing said analog image signal and providing a processed image signal at internal node;

an ADC unit (118) for converting said processed image signal into a digital image signal.

Figure 1 of Obie does not show a clamping circuit connecting between said internal node and a reference level and the filter is adjustable. Figures 3 and 4 of Peterson show a clamping circuit (131) for clamping the node voltage with a reference voltage during clamping interval for enhancing the signal to noise ratio (col. 60-65) Therefore, it would have been obvious to one of ordinary skill in the art to implement the clamping circuit taught by Peterson to the circuit of Obie for enhancing the signal to noise ratio. Figure 1 of Obie does not show that the low-pass filter (112) is an adjustable filter for providing a bandwidth adjustable in response to the display resolution such that the greater the display resolution. . Figure 1of Belkin shows a video circuit receiving image signal having an adjustable filter (2) for providing a bandwidth adjustable in response to the display resolution such that the greater the bandwidth, the greater the display resolution (col.1 lines 40-67). Therefore, it would have been obvious to on of ordinary skill in the art to. Therefore, it would have been obvious to one of ordinary skill in the art to replace the adjustable filter (112) of Obie with the adjustable filter (2) of Belkin for providing a bandwidth adjustable in response to the display resolution such that the greater the bandwidth, the greater the display resolution.

Regarding claim 8, the combination of Obie, Peterson and Belkin includes all the limitations of claim 8 except for the limitation that the low pass filter (112) of Obie comprises a variable resistor. Note that the low-pass filter of the present application in figures 2 and 3 of the present application is a simple low-pass filter comprising two elements: a variable resistor and a capacitor. One of ordinary skill in the art know that a low-pass filter is used in any analog circuit including video circuit for eliminating unwanted frequencies or to vary the resolution of the display (See US 6,606,171; US 6,738,087). The bandwidth of the low-pass filter depends on the (R-C) values of the resistor and the capacitor that determine the cut-off frequency or the bandwidth of the low-pass filter. As discussed above, figure 3 of Kanagawa shows a simple low-pass filter (211), similar to the simple low-pass filter low-pass filter (24) of the present application in figures 2 and 3 of the present application, comprising a variable resistor (2111) and (2112) for varying the bandwidth of the low-pass filter thus, the resolution of the analog signal or the video signal is adjustable (smaller or greater). Therefore, it would

have been obvious to one of ordinary skill in the art to consider that the adjustable filter (112) of Obie comprises a variable resistor as taught by Kanagawa for varying the bandwidth of the filter.

Regarding claims 9 and 10, the clamping circuit (131) taught by Peterson (131) for clamping the node voltage with a reference voltage during clamping interval for enhancing the signal to noise ratio (col. 60-65) comprises a transistor (M9) having a drain connected to the internal node and a source connected to a reference level.

Regarding claims 11 and 12, the combination of Obie, Peterson, Belkin and Kanagawa includes all the limitation of claim 10 except for the limitation that the clamping circuit comprises a variable resistor and a transistor. Figure 1 of Kwon shows a clamping circuit comprising a variable resistor (N1) control by signal (Vbias) and a clamping transistor (N2) controlled by signal (clamp_en) for adjusting the voltage at the internal node (col. 5, lines 12-33). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the clamping circuit taught by Kwon to the circuit of Obie for adjusting the voltage at the internal node. The connections of these two components are clearly shown in figure 1 of Kwon.

Response to Arguments

In the Remarks, the core of the argument is that **only** the low-pass filter of the present application has an ability to provide a bandwidth adjustable in response to the display resolution such that the greater the display resolution, the greater the bandwidth. The circuit of claim 1 is a simple circuit that can be found in any textbook. Figures 2 and 3 of the present application show that the simple filter circuit comprises a variable resistor and a capacitor. One of ordinary skill in the art knows that the low-pass filter basically filters out the unwanted high frequencies or high frequency noises. By varying the value of the resistor (RC value), the bandwidth of the filter varies. The bandwidth of the filter contents a spectrum of frequencies i.e., a range of information including video display information. By varying the bandwidth of the filter the display resolution varies. Therefore, this is an inherent feature of any adjustable filter. The Applicant relies on the language of the claim, without considering the structure of the claimed circuit: an adjustable filter comprising only a variable resistor and a capacitor, to

distinguish the claimed circuit over the prior art. The Applicant is requested to prove that the low-pass filter (211) comprising an adjustable resistor (2111) and a capacitor (2112) in figure 3 of Kanagawa which is identical to the claimed filter circuit (24) comprising a variable resistor (Rf) and a capacitor (Cf) in figure 3 of the present application cannot perform the same function as the claimed circuit. Unless the Applicant can prove that, by some specific reasons, only the claimed filter circuit can perform the claimed function, any identical filter comprising an adjustable resistor and a capacitor can also perform the claimed function.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen
08-29-06

TUAN T. LAM
PRIMARY EXAMINER